WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit, comprising:

a first pad mounted on a main surface of a semiconductor substrate;

a second pad mounted on the main surface and positioned adjacent to the first pad;

a pad joint mounted between the first pad and the second pad to connect the first pad and the second pad;

a first signal input/output circuit including a first output buffer connected to the first pad;

a second signal input/output circuit including a second input buffer connected to the second pad, and a second output buffer connected to the second pad and including an output section having a controllable output impedance; and

an input/output signal control circuit connected to the first signal input/output circuit and the second signal input/output circuit;

wherein the input/output signal control circuit includes a first latch circuit connected to an input section of the first output buffer, a second latch circuit connected to an output section of the second input buffer, and a control switch connected to an input section of the first output buffer and an input section of the second output buffer.

2. The semiconductor integrated circuit according to claim 1, wherein the first pad and the second pad have substantially a same width, and the pad joint has a same width as the first pad and the second pad and connects the first pad and the second pad.

3. The semiconductor integrated circuit according to claim 1, further comprising a second control switch constituting the controllable output impedance;

wherein the output section of the second output buffer is connected to the second pad and the second input buffer via the second control switch.

4. The semiconductor integrated circuit according to claim 1, wherein the second output buffer is a tristate buffer.

5. The semiconductor integrated circuit according to claim 1, the semiconductor integrated circuit operating in a normal operation mode or a test mode, wherein in the normal operation mode the first output buffer generates an output signal while the output impedance is set to high with the first control switch turned OFF; and in the test mode the first output buffer and the second output buffer simultaneously generate output signals having the same logic level while the output impedance is set to low with the first control switch turned ON.

6. The semiconductor integrated circuit according to claim 1, the semiconductor integrated circuit operating in a normal operation mode or a test mode, wherein in the normal operation mode the first output buffer generates an output signal while the output impedance is set to high with the first control switch turned OFF; and in the test mode the first latch circuit latches a signal input to the first output buffer with specified timing and latches an signal output from the second input buffer by the second latch circuit with specified timing while the output impedance is set to high with the first control switch turned OFF.

7. The semiconductor integrated circuit according to claim 1, the semiconductor integrated circuit operating in a normal operation mode, a first test mode, or a second test mode, wherein in the normal operation mode the first output buffer outputs an output signal while the output impedance is set to high with the first control switch turned OFF; in the first test mode the first output buffer and the second output buffer simultaneously generate output signals having the same logic level while the output impedance is set to low with the first control switch turned ON; in the second test mode the first latch circuit latches a signal input to the first output buffer with specified timing and the second latch circuit latches an signal output from the second input buffer with specified timing while the output impedance is set to high with the first control switch turned OFF.

8. The semiconductor integrated circuit according to claim 6, wherein the input/output signal control circuit further includes a comparator circuit for comparing the output signals of the first latch circuit and second latch circuit.

9. The semiconductor integrated circuit according to claim 7, wherein the input/output signal control circuit further includes a comparator circuit for comparing the output signals of the first latch circuit and second latch circuit.

10. A semiconductor integrated circuit, comprising:

a first pad mounted on a main surface of a semiconductor substrate;

a second pad mounted on the main surface and positioned adjacent to the first pad;

a pad joint mounted between the first pad and the second pad to connect the first pad and the second pad;

a first signal input/output circuit including a first output buffer connected to the first pad;

a second signal input/output circuit including a second output buffer;

an output section of the second output buffer connected to the second pad and having a controllable output impedance; and

an input/output signal control circuit connected to the first signal input/output circuit and the second signal input/output circuit;

wherein the input/output signal control circuit includes a first control switch connected between an input section of the first output buffer and an input section of the second output buffer; in a normal operation mode the first output buffer generates an output signal while the output impedance is set to high with the first control switch turned OFF; and in a test mode the first output buffer and the second output buffer simultaneously generate output signals having the same logic level while the output impedance is set to low with the first control switch turned ON.

11. A semiconductor integrated circuit, comprising:

a first pad mounted on a main surface of a semiconductor substrate;

a second pad mounted on the main surface and positioned adjacent to the first pad;

a pad joint mounted between the first pad and the second pad to connect the first pad and the second pad;

a first signal input/output circuit including an output buffer connected to the first pad;

a second signal input/output circuit including a second input buffer connected to the second pad; and

an input/output signal control circuit connected to the first signal input/output circuit and the second signal input/output circuit;

wherein the input/output signal control circuit includes a first latch circuit and a second latch circuit; an input section of the first latch circuit is connected to an input section of the first output buffer; an input section of the second latch circuit is connected to an output section of the second input buffer; in a normal operation mode the first output buffer generates an output signal; and in a test mode the first latch circuit latches a signal input to the first output buffer with specified timing and the second latch circuit latches a signal output from the second input buffer with specified timing.

12. The semiconductor integrated circuit according to claim 11, wherein the input/output signal control circuit includes a comparator circuit for comparing the output signals of the first latch circuit and the second latch circuit.